VIETNAM NATIONAL UNIVERSITY, HANOI
VNU UNIVERSITY OF ENGINEERING AND TECHNOLOGY

SOCIALIST REPUBLIC OF VIETNAM
Independence – Freedom – Happiness

INFORMATION ON DOCTORAL THESIS

1. Full name : Nguyen Duy Anh 2. Sex: Male

3. Date of birth: 07 May, 1990 4. Place of birth: Ha Noi

5. Admission decision number: 1222/QĐ-CTSV Dated 06 Dec, 2017

6. Changes in academic process:

Extend the study period according to Decision No. 65/QD-DT dated January 22, 2021, issued by the Rector of the University of Technology, Vietnam National University, Hanoi.

Adjustment of supervisors according to Decision No. 435/QD-DT dated June 1, 2021, issued by the Rector of the University of Technology, Vietnam National University, Hanoi.

7. Official thesis title: Algorithms and Hardware Architectures for high efficient Spiking Neural Networks

8. Major: Electronic Engineering 9. Code: 9510302.01

10. Supervisors: Assoc. Prof. Xuan-Tu Tran

Prof. Francesca Iacopi

11. Summary of the **new findings** of the thesis:

Firstly, the dissertation proposes a simple digital design for the Integrate-and-Fire (IF) neuron model. The design focuses on minimizing features compared to other works, resulting in a 3.2 times reduction in the implementation's spatial cost compared to other designs. To test the effectiveness of the design at a system level, the dissertation also proposes a hardware design for a feedforward Spiking Neural Network (SNN) with 3 layers for the MNIST application. The SNN is trained using the conversion algorithm from Artificial Neural Network (ANN) to SNN, and the network's weights are quantized in 10-bit fixed-point format.

Secondly, the dissertation proposes a novel algorithm for training SNNs with ternary weight representation. Such SNNs are referred to as Ternary Weight Spiking Networks

(TW-SNNs). The goal of TW-SNNs is to reduce memory storage requirements for the network weights. To demonstrate the energy efficiency of the proposed method, the dissertation also presents a hardware design for the TW-SNN network.

Thirdly, the dissertation proposes a new max-pooling method for Convolutional SNNs. The proposed pooling method ensures the accuracy of the SNN while still being easily implementable on hardware.

12. Practical applicability, if any:

The current applications of artificial intelligence and deep learning are being widely deployed in various aspects of our lives. However, the deployment of deep learning applications onto edge devices faces challenges due to high energy consumption and memory storage requirements. Spiking Neural Networks (SNNs) offer an efficient solution for deploying AI applications on edge devices. The dissertation focuses on proposing hardware solutions (such as designing a simplified neuron model and network architecture) and software solutions (such as designing algorithms to reduce memory requirements).

13. Further research directions, if any:

- Develop a 3D-NoC model to integrate into the hardware design for SNNs, enabling scalability for large-scale SNN network models.
- Utilize advanced memory technologies such as memristors to design hardware for SNNs.

14. Thesis-related publications:

- Duy-Anh Nguyen, Duy-Hieu Bui, Francesca Iacopi, Xuan-Tu Tran, ”An Efficient Event-driven Neuromorphic Architecture for Deep Spiking Neural Networks” 2019 32nd IEEE International System-on-Chip Conference (SOCC 2019), pp. 144-149, Sep 2019, Singapore, ISBN: 978-1-7281-3282-6.

- Duy-Anh Nguyen, Xuan-Tu Tran, Khanh N. Dang, Francesca Iacopi, ”A lightweight max-pooling method and architecture for deep spiking convoultional neural networks”, 2020 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS 2020), pp. 209-212, Dec 2020, Halong Bay, Vietnam, ISBN: 978-17281-9396-0.

- Duy-Anh Nguyen, Xuan-Tu Tran, Francesca Iacopi, ”A review of algorithms and hardware implementations for spiking neural networks”, Journal of Low Power Electronics and Applications, Apr. 2021, Vol. 11, 23, ISSN: 2079-9268 (ESCI, Q2).

- Duy-Anh Nguyen, Xuan-Tu Tran, Khanh N. Dang, Francesca Iacopi, ”A low-power, high-accuracy with fully on-chip ternary weight hardware architecture for Deep Spiking Neural Networks”, Microprocessors and Microsystems, Vol. 90, 2022 104458, ISSN: 0141-9331 (SCIE, Q2).